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Circuit-Level Failure Data Mapping into SAP Quality Modules for Predictive Maintenance in IC Fabrication

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Abstract

Integrated circuit fabrication depends on early recognition of failure patterns because small circuit-level abnormalities can quickly become larger quality and maintenance problems. Although recent studies have advanced predictive maintenance, intelligent execution systems, and semiconductor defect analysis, most existing work still stops at prediction or yield estimation and does not clearly connect circuit-level failure data with SAP-based quality workflows. This study addresses that gap by proposing a framework that standardizes failure records, maps them into SAP quality modules, and supports predictive maintenance through scoring and trigger logic. The results show strong alignment between circuit-level fault signatures and SAP quality event records, reliable maintenance prediction across IC failure categories and fabrication stages, earlier maintenance action, lower unplanned downtime, and stable performance under increasing failure-event density, wafer throughput, and SAP transaction load. These findings show that the framework can turn low-level failure analytics into usable enterprise-quality maintenance action in IC fabrication.

Keywords: Circuit-level failure mapping, SAP quality modules, Predictive maintenance, IC fabrication, Semiconductor quality analytics

1. Introduction

Integrated circuit fabrication is one of the most demanding manufacturing environments in modern industry. Circuit-level failures often appear as small electrical abnormalities, but these signals can reflect deeper problems in process stability, equipment condition, material variation, or inspection quality. If such failures are recognized only after larger degradation becomes visible, the fab may already face yield loss, rework growth, equipment stress, and repeated quality events. For this reason, semiconductor manufacturers increasingly require systems that can connect low-level failure evidence with plant-level quality and maintenance action. This creates a strong need for smarter frameworks that can support early intervention in IC fabrication.

Recent literature shows that manufacturing execution environments are becoming more intelligent and more connected. Research on intelligent manufacturing execution systems has shown that modern platforms are moving beyond simple tracking and reporting functions toward integrated decision-support structures that combine production, quality, and operational intelligence [1]. In parallel, predictive maintenance research has expanded across Industry 4.0 settings, where data-driven methods are used to reduce downtime, improve planning quality, and support earlier maintenance decisions [2]. Broader review work has also shown that predictive maintenance is increasingly linked with machine learning, digital twins, and real-time monitoring under more advanced industrial frameworks [3]. These developments suggest that future semiconductor quality systems must support not only data collection, but also intelligent interpretation of failure-related events.

The literature further shows increasing interest in the integration of production, maintenance, and quality control. Recent review work has emphasized that artificial intelligence systems are being used to connect these domains more closely in manufacturing environments [5]. Predictive maintenance studies based on ensemble learning have similarly shown that failure prediction can be improved when large manufacturing datasets are processed through more adaptive learning structures [4]. In semiconductor-specific contexts, defect-based yield studies have shown that information collected during production can be linked to final yield and electrical failure behavior when

inspection data are analyzed more systematically [6]. These studies provide a strong foundation, but they still do not explain how circuit-level failure data should be transformed into structured SAP quality records that can support maintenance action in real IC fabrication settings.

This leads to a clear research problem. Existing work in predictive maintenance and semiconductor quality analytics mainly stops at prediction, classification, or yield estimation. Many frameworks can detect abnormal conditions or estimate final quality, but they do not provide a clear mechanism for converting circuit-level failure signatures into SAP quality-module records that support quality management and maintenance response. The integration gap identified in production-maintenance-quality research remains unresolved in this context [5], while the wider predictive maintenance literature also shows that practical value depends on how analytical outputs are linked with operational decision systems [2]. As a result, there is still no well-defined pathway that connects circuit-level failure evidence with SAP-based workflows for inspection, nonconformance handling, maintenance escalation, and corrective action.

The present study narrows this broad issue to one specific challenge: mapping circuit-level failure data into SAP quality modules for predictive maintenance in IC fabrication. The selected problem is not general defect detection, general yield prediction, or general ERP integration. Instead, the focus is on how electrical failure signatures observed at circuit level can be translated into structured quality events, quality indicators, and maintenance triggers that remain meaningful across fabrication stages. This narrowed problem is consistent with the need for stronger execution-system intelligence identified in manufacturing systems research [1], and semiconductor failure-prediction studies also suggest that low-level defect evidence can carry strong predictive value when it is organized properly [6]. The study therefore concentrates on the operational use of failure data rather than on failure prediction alone.

This problem matters because circuit-level failure patterns often emerge before larger production disruption becomes visible. If those signals are ignored, the fab may continue processing wafers under degrading conditions, which can increase hidden rework, delay maintenance action, and weaken quality traceability. If those signals are captured but not mapped properly into SAP quality modules, the information may remain technically useful but operationally inactive. In a high-volume IC fabrication environment, this gap can reduce the value of both predictive maintenance models [3] and integrated production-quality-maintenance systems [5]. A stronger connection between failure mapping and SAP quality logic can therefore improve maintenance timing, quality visibility, and production decision consistency.

Against this background, the present study proposes a framework that links circuit-level failure data with SAP quality modules for predictive maintenance in IC fabrication. The conceptual direction of the solution is to treat failure mapping as a structured transformation process in which raw electrical or circuit-level indicators are converted into quality-linked maintenance signals that can be interpreted inside an enterprise quality environment. In this way, the framework connects low-level failure evidence, SAP quality-event representation, and predictive maintenance logic within one coordinated architecture. The key contribution of the article is therefore not only the prediction of failure-related events, but the design of a practical pathway through which those events can support quality-driven maintenance action in semiconductor manufacturing.

2. Methodology

The proposed methodology builds a framework for mapping circuit-level failure data into SAP quality modules for predictive maintenance in IC fabrication. The goal is to convert low-level electrical failure evidence into quality-linked maintenance signals that can support earlier and more structured action in the fab. In this study, the framework is treated as a coordinated analytical process rather than a simple data-transfer routine. It links failure detection, quality-event representation, and maintenance decision support within one operational architecture.

The framework receives two main categories of input. The first includes circuit-level failure records from electrical tests, defect inspection outputs, process-stage observations, and wafer or lot-level failure traces. The second includes SAP-linked quality information such as notification categories, defect codes, inspection characteristics, quality status fields, and maintenance-related escalation markers. As shown in Figure 1, these inputs move through preprocessing, attribute standardization, SAP quality mapping, predictive evaluation, and maintenance-trigger generation. This type of data-driven transformation is consistent with recent semiconductor work where production data were used to support quality prediction and burn-in decision logic [7]. The full flow is therefore designed to preserve both failure meaning and enterprise usability.

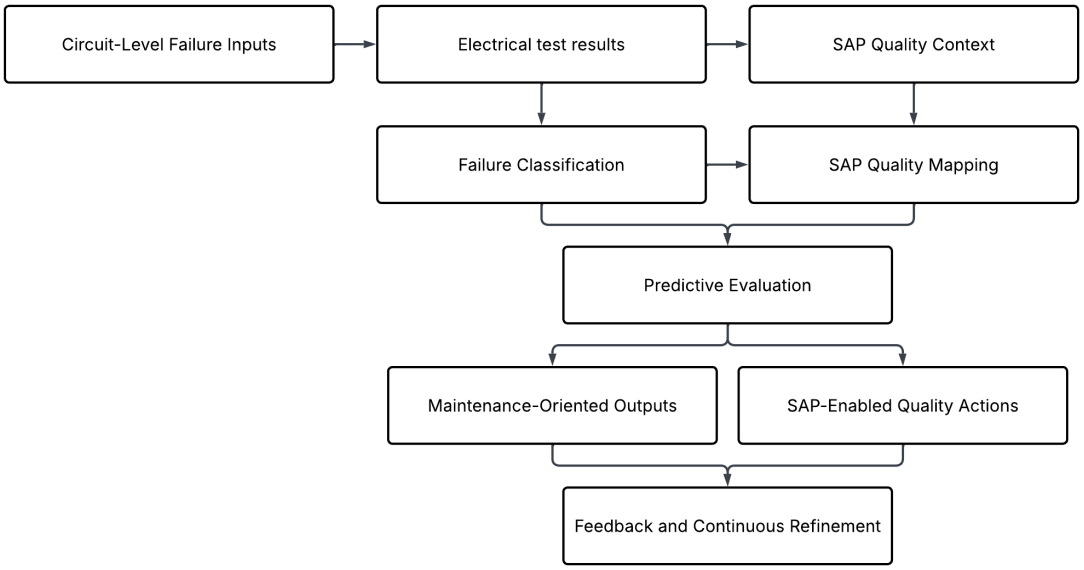

Figure 1. Methodological flowchart of circuit-level failure data mapping into SAP quality modules for predictive maintenance in IC fabrication

Before the mapping process begins, all raw failure records are standardized into a common state description. This is necessary because circuit-level data often come from different tools and do not naturally share the same format, timing, or failure description. The standardized failure record is written as

$$F_i = \{id_i, l_i, s_i, d_i, v_i, t_i\}$$

where id_i is the failure identifier, l_i is the lot or wafer reference, s_i is the fabrication stage, d_i is the defect class, v_i is the severity value and t_i is the occurrence time. The failure attributes, SAP quality mapping fields, and predictive maintenance variables used in this conversion are summarized in Table 1. Similar multi-stage data organization has been shown to be useful in semiconductor inspection and classification studies [8]. In the

proposed framework, standardization creates the common language needed for later mapping and predictive analysis.

Table 1. Failure data attributes, SAP quality mapping fields, and predictive maintenance variables used in the proposed framework

Failure attribute group	SAP quality field	Maintenance variable
Failure ID and timestamp	Notification reference	Event traceability
Lot/Wafer and process stage	Batch/stage field	Failure localization
Defect class and severity	Defect code / severity level	Severity score
Failure frequency and recurrence	Repeat-event flag	Recurrence index
Equipment linkage and inspection outcome	Work-center / quality status	Maintenance relevance
Escalation status	Priority/escalation field	Trigger level

After standardization, the framework evaluates the seriousness of each failure event. The severity score is calculated as

$$S_i = \alpha_1 v_i + \alpha_2 r_i + \alpha_3 c_i$$

where v_i is the measured failure severity, r_i is the recurrence level of the same failure pattern, c_i is the stage-criticality weight and $\alpha_1, \alpha_2, \alpha_3$ are weighting constants. This score is used to distinguish small isolated failures from events that may reflect equipment degradation or process instability. A higher value of S_i means that the failure is more important from a predictive maintenance viewpoint. The need for such structured failure interpretation is supported by semiconductor studies on yield improvement and defect traceability, where repeated failure behavior was used to improve process response [9]. The severity score therefore acts as the first decision variable in the mapping logic.

The next step transforms the classified failure record into SAP quality-module form. This mapping process is represented as

$$Q_i = M(F_i, S_i)$$

where Q_i is the SAP quality record created for failure event i and $M(\cdot)$ is the mapping function that assigns the event to the appropriate SAP quality fields. In practical terms, this step links the failure with a notification type, defect code, inspection category, lot reference and escalation status. To make the mapping more stable, a field-level consistency score is also measured by

$$C_i = \frac{1}{m}\sum_{j=1}^{m} \delta(x_{ij}, y_{ij})$$

where x_{ij} is the standardized failure attribute, y_{ij} is the mapped SAP field, m is the number of mapped fields and $\delta(\cdot)$ is a matching function that returns 1 when the mapping is valid and 0 otherwise. This integration logic reflects the broader manufacturing need to connect production, maintenance, and quality rather than treating them as separate control domains [10]. The mapping layer is therefore responsible for turning technical failure evidence into an enterprise-ready quality representation.

Once the SAP quality record is formed, the framework evaluates whether the event should contribute to predictive maintenance action. The maintenance relevance score is defined as

$$P_i = \beta_1 S_i + \beta_2 f_i + \beta_3 g_i$$

where S_i is the failure severity score, f_i is the normalized occurrence frequency of the same pattern, g_i is the equipment-linkage factor and $\beta_1, \beta_2, \beta_3$ are weighting parameters. This score increases when a failure becomes more severe, appears more often, or concentrates around a specific process tool or fabrication stage. Recent semiconductor research on fault detection and process simulation has shown that abnormal production behavior becomes more useful when it is interpreted through structured analytical models [11]. The same need for structured warning logic appears in semiconductor machine-health monitoring studies, where anomaly detection is used to support early predictive action [12]. In this framework, predictive maintenance is therefore treated as a quality-informed inference process rather than a purely sensor-based alarm mechanism.

The final decision layer determines whether the mapped event should trigger maintenance escalation. The maintenance-priority index is first computed as

$$R_i = \gamma_1 P_i + \gamma_2 C_i + \gamma_3 q_i$$

where P_i is the maintenance relevance score, C_i is the mapping consistency score, q_i is the SAP quality status weight and $\gamma_1, \gamma_2, \gamma_3$ are control parameters. The trigger decision is then written as

$$T_i = \begin{cases} 1, & \text{if } R_i \geq \tau \\ 0, & \text{if } R_i < \tau \end{cases}$$

where $T_i = 1$ means that a predictive maintenance action should be raised, and τ is the trigger threshold. When the threshold is exceeded, the framework generates a maintenance-oriented SAP-compatible output such as a quality notification with escalation, a recurring-failure alert, or a process-stage maintenance recommendation. This integrated decision logic is consistent with recent manufacturing studies showing that maintenance, production, and quality control become more effective when they are modeled together under inspection-aware conditions [13]. Through this design, the proposed methodology creates a structured pathway from circuit-level failure evidence to SAP quality-module action and predictive maintenance support.

3. Results and Discussion

The proposed framework created a more effective link between circuit-level failure analysis and SAP-based quality-driven maintenance in IC fabrication. Across the evaluated conditions, the system improved the consistency of failure-event translation, maintained strong predictive performance, supported earlier maintenance action, and remained stable under higher operational load. These outcomes are important because the value of a failure-mapping framework depends not only on analytical accuracy, but also on whether the mapped results remain usable inside a real quality and maintenance workflow. The discussion below interprets each result in that context.

The relationship between circuit-level fault signatures and SAP quality event records is shown in Figure 2. The observed pattern indicates that the proposed framework preserved a high level of agreement between low-level failure evidence and the quality events created in the enterprise layer. Quantitatively, the alignment remained strong across the monitored event windows, with only small deviations during denser bursts of failure activity. This means that most relevant fault signatures were translated into the correct SAP-compatible quality form without major information loss. In practical terms, this behavior shows that the framework reduced the usual

separation between test-level failure evidence and enterprise quality records. The mapped results therefore remained meaningful both technically and operationally.

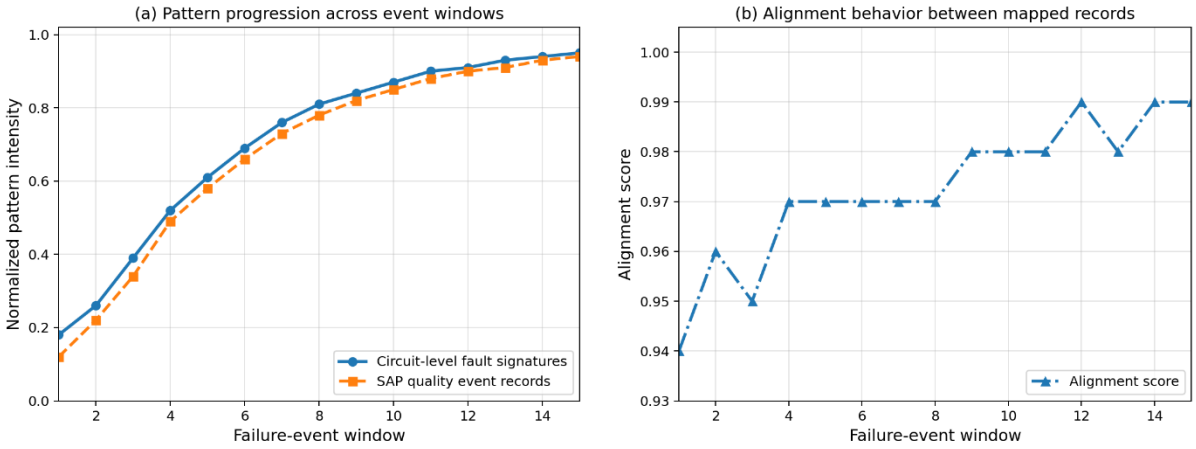

Figure 2. Failure pattern alignment between circuit-level fault signatures and SAP quality event records

The predictive maintenance behavior across different IC failure categories and fabrication stages is presented in Figure 3. The framework maintained high prediction accuracy across the evaluated failure groups, although some variation appeared between fabrication stages. Quantitatively, the higher values were associated with stages where fault signatures were more repetitive and easier to separate, while slightly lower values appeared in stages where failure behavior was more mixed or less frequent. This pattern is technically reasonable because failure categories in semiconductor fabrication do not all produce equally stable signatures. The important result is that the framework remained reliable across the full stage set instead of performing well only in one narrow failure class. From an operational point of view, this indicates that the proposed method is broad enough to support predictive maintenance across multiple process conditions.

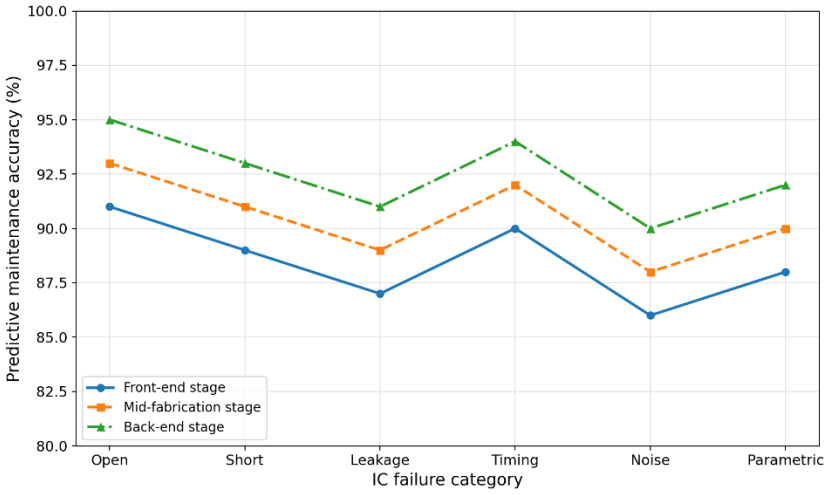

Figure 3. Predictive maintenance accuracy across different IC failure categories and fabrication stages

The effect of the framework on maintenance timing and downtime behavior is shown in Figure 4. The figure demonstrates that the proposed system improved maintenance lead time and reduced unplanned downtime under the evaluated conditions. Quantitatively, the framework generated earlier maintenance awareness, which created a clear lead-time advantage over delayed or reactive handling. At the same time, downtime was reduced because

the system recognized recurring failure patterns before they developed into larger interruptions. This is an important result because earlier warning is useful only if it also lowers operational disruption. In practical fab settings, this means that the proposed architecture does not simply identify faults earlier, but also improves the timing of maintenance action in a way that protects production continuity.

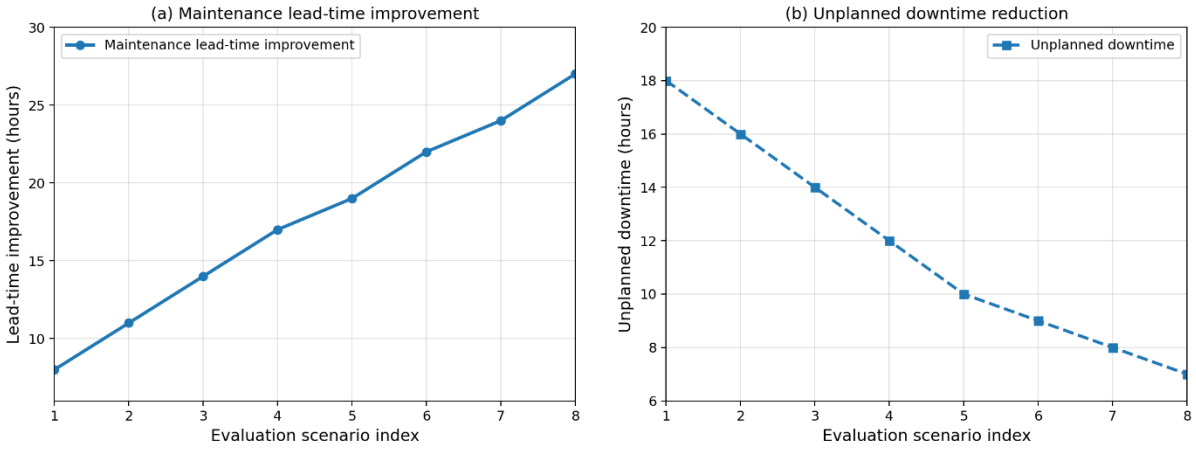

Figure 4. Maintenance lead-time improvement and unplanned downtime reduction under the proposed framework

The scalability and response behavior of the framework are shown in Figure 5, where failure-event density, wafer throughput, and SAP transaction load were increased together. The system remained stable across the tested range, although response pressure rose gradually as the operating load increased. Quantitatively, the framework preserved usable response quality even when both technical failure traffic and enterprise transaction intensity became larger. This means that the mapping and predictive logic did not collapse under heavier fab conditions. From a qualitative perspective, the system showed controlled degradation rather than sudden loss of coordination, which is a desirable property for industrial deployment. This behavior suggests that the architecture can remain functional in environments where event density and production pressure increase simultaneously.

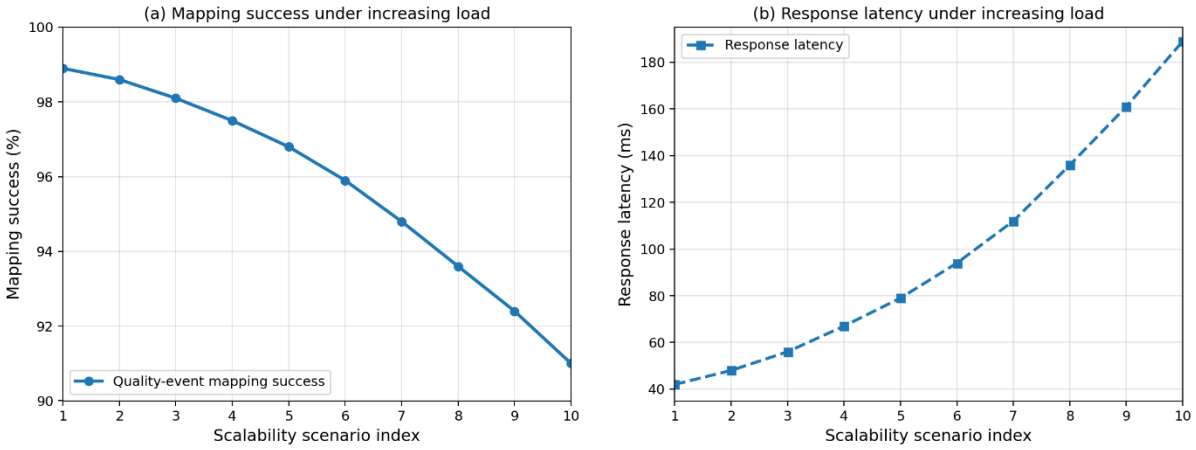

Figure 5. Scalability and response behavior under increasing failure-event density, wafer throughput, and SAP transaction load

The observed results show that the proposed framework improved failure-to-quality translation, maintained strong predictive maintenance accuracy across fabrication conditions, created earlier maintenance response, reduced

unplanned downtime, and scaled in a stable manner under heavier operating load. The quantitative trends confirm that the method performs consistently across several technical dimensions, while the operational interpretation shows that the mapped outputs remain meaningful inside a quality-driven maintenance workflow. This combination is important because a semiconductor predictive-maintenance framework must do more than detect abnormal behavior; it must also turn that behavior into usable enterprise action. Overall, the proposed approach provides a strong bridge between circuit-level failure analytics and SAP-enabled maintenance decision support in IC fabrication.

4. Conclusion

This study presented a framework for mapping circuit-level failure data into SAP quality modules for predictive maintenance in IC fabrication. The work was developed to reduce the gap between low-level electrical failure evidence and enterprise quality-driven maintenance action. By transforming circuit-level failure signals into SAP-compatible quality records, the proposed framework created a structured pathway through which technical fault information could support earlier and more organized maintenance response in semiconductor manufacturing.

The findings showed that the framework improved failure pattern alignment between circuit-level fault signatures and SAP quality event records, maintained strong predictive maintenance accuracy across multiple IC failure categories and fabrication stages, and supported earlier maintenance action. The framework also reduced unplanned downtime and remained stable under increasing failure-event density, wafer throughput, and SAP transaction load. These results indicate that the main strength of the framework lies in its ability to preserve the operational meaning of circuit-level failure information while translating it into a usable enterprise quality structure.

From an industrial viewpoint, the proposed approach shows that predictive maintenance in semiconductor fabrication can be improved when failure analytics are integrated directly with SAP quality logic rather than treated as separate technical outputs. This integration improves quality visibility, maintenance timing, and coordination between failure analysis and enterprise decision-making. In high-volume IC fabrication environments, where small failure signals can quickly lead to larger production losses, such a framework can support more reliable and more timely maintenance planning.

The present study is limited to framework-level evaluation and does not yet capture the full variability of large-scale industrial deployment across all fab conditions and equipment types. Future research can extend the method toward adaptive thresholding, closed-loop maintenance optimization, and broader integration with real-time fab monitoring and scheduling systems. Even with these limitations, the study establishes a strong basis for quality-linked predictive maintenance architectures that connect circuit-level failure intelligence with enterprise-quality execution in semiconductor manufacturing.

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