



# **AI-Assisted Fault Localization in Complex PCB Layouts Using Graph-Based Signal Path Analysis**

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## Abstract

Printed circuit boards are essential to modern electronic systems, but fault localization becomes harder as layouts grow denser and more interconnected. A local defect can affect multiple connected paths, making the true electrical fault difficult to identify through visual inspection alone. Recent studies have improved PCB defect detection using AI-based inspection models, but most of them still focus on visible defect identification rather than true fault-source localization. To address this gap, this article presents an AI-assisted fault localization framework based on graph-based signal path analysis. The method converts PCB layouts into graph representations, evaluates signal path consistency, measures path deviation, aggregates regional fault likelihood, and ranks candidate fault regions using AI support. The results show that the framework provides better fault-source separation, stronger ranking stability, and better robustness under noise, dense routing, and increasing graph complexity than baseline approaches. These findings show that graph-guided signal reasoning offers a more reliable basis for PCB diagnosis. The proposed framework can support automated inspection, debugging, repair guidance, and reliability assessment in advanced electronic systems.

**Keywords:** Printed circuit boards, fault localization, graph-based signal path analysis, AI-assisted diagnosis, PCB inspection, signal path consistency

## 1. Introduction

Printed circuit boards are the physical and electrical core of modern electronic systems. They carry signals, distribute power, connect components, and support the overall functional behavior of devices used in communication, computing, sensing, automotive control, and embedded electronics. As PCB layouts become denser, multilayered, and more compact, fault localization becomes increasingly difficult. A local defect such as a broken trace, weak via, solder bridge, pad damage, or interconnect discontinuity can influence a much larger routing region and generate abnormal responses far from the actual source of failure. For this reason, fault localization in advanced PCB layouts is no longer only a visual inspection problem [1]. It is also a structural and electrical reasoning problem that requires understanding how connectivity is organized and how signal paths are altered when part of the layout is damaged.

Recent literature shows major progress in AI-supported PCB inspection, especially in defect detection, classification, and efficient visual analysis. Multi-scale attention-based models have improved the detection of small and irregular PCB defects by strengthening feature extraction across different spatial levels [1]. Key-point localization methods have improved the identification of fine defect positions that are often difficult to isolate with standard region detectors [2]. Region-based convolutional approaches have shown reliable performance in detecting and classifying common PCB fault categories under complex image conditions [3]. Small-sample high-precision models have addressed the practical problem of limited defect data and improved sensitivity to subtle local abnormalities [4]. Lightweight frameworks have reduced computational burden and made automated inspection more suitable for real-time or resource-limited settings [5]. Transformer-based models have further improved feature representation and robustness for tiny defect patterns in complex backgrounds [6]. Although these studies have clearly advanced PCB inspection, their main strength remains visual recognition. They are

highly effective at identifying whether a suspicious region exists, but they provide limited insight into how that region relates to electrical connectivity, routing dependency, and fault propagation across the board.

This creates an important research gap. Most existing methods remain image-centered and treat PCB faults mainly as appearance-level abnormalities. In practice, however, many PCB failures are not purely local visual events. A visible anomaly may be only one symptom of a larger connectivity problem, while the true electrical fault may lie upstream, downstream, or across another connected branch. In dense layouts, the region that looks defective and the region that actually causes signal failure may not be the same [3]. Even high-accuracy methods that improve local defect recognition still do not model routing dependencies in a way that supports electrical fault tracing [4]. Lightweight models improve screening speed, but not structural interpretation [5]. Transformer-based methods improve feature learning, but they still operate mainly at the level of image-based defect identification rather than graph-level path reasoning [6]. The main problem, therefore, is the absence of a topology-aware and signal-aware framework that can localize faults by reasoning over connectivity structure instead of only detecting visible defect regions.

To address this gap, the present study focuses on AI-assisted fault localization in complex PCB layouts using graph-based signal path analysis. The key idea is to move from image-only reasoning to graph-based electrical reasoning. In the proposed view, pads, vias, junctions, and component pins are represented as nodes, while traces and conductive links are represented as edges. This graph abstraction makes it possible to model the PCB as an interconnected signal network and to analyze how expected paths are broken, diverted, weakened, or interrupted by faults. Such a representation is more suitable for complex layouts where behavior depends strongly on interconnect structure, branching relationships, and route continuity [2]. It is also more effective when the effect of a fault appears across several connected regions instead of one isolated visible location [4]. This problem matters because weak fault localization increases test time, raises repair cost, and can lead to unnecessary replacement of healthy components. In practical settings, engineers need not only to know that a defect exists, but also where the most likely electrical source of failure is located [1].

The conceptual direction of this work is to combine graph-based signal reasoning with AI-assisted decision support for more reliable PCB fault localization. The PCB layout is first transformed into a graph so that connectivity can be studied in a formal topological form. Expected signal paths are then traced across this graph, and abnormal path behavior is used to identify likely fault regions. AI is used not only as a detector, but as an assisting layer that evaluates disrupted path patterns, ranks candidate fault locations, and improves localization confidence in dense and ambiguous routing environments. Based on this direction, the study contributes a graph-based representation of complex PCB layouts for fault analysis, a signal-path-centered strategy for identifying likely fault regions, and an AI-assisted localization framework designed for dense routing environments where image-level inspection alone is not sufficient.

## 2. Methodology

The proposed methodology localizes faults in complex PCB layouts by combining graph-based signal path analysis with AI-assisted ranking. The workflow shown in Figure 1 starts from PCB layout parsing and feature extraction, then moves to graph construction, signal path modeling, path anomaly estimation, regional fault

scoring, and final candidate ranking. The purpose of this design is to move beyond visual defect detection and toward electrical fault localization based on connectivity behavior. In this framework, the PCB is not treated only as an image. It is treated as an interconnected signal network in which structural relations, routing continuity, and local abnormalities are analyzed together before a final localization decision is made.

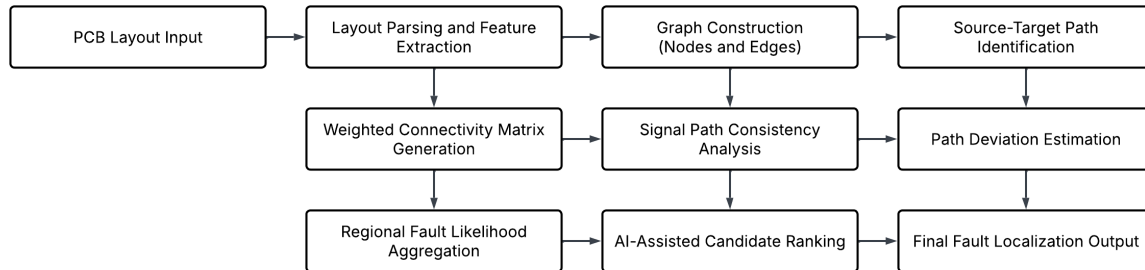


Figure 1. Workflow of the proposed graph-based signal path analysis and AI-assisted fault localization framework

The first stage is PCB graph construction. The layout is parsed so that pads, vias, junctions, and component pins become graph nodes, while traces, conductive bridges, and routing segments become graph edges. This graph transformation is consistent with graph-based circuit modeling methods that represent electrical systems through topological structures [7]. It also agrees with graph-oriented circuit extraction methods in which connectivity is reconstructed from layout or schematic information [8]. If the PCB graph is written as  $G$ , then

$$G = (V, E, X_n, X_e) \quad (1)$$

where  $V$  is the set of nodes,  $E$  is the set of edges,  $X_n$  is the node feature matrix, and  $X_e$  is the edge feature matrix. In this work, node features include element type, geometric position, layer index, and local degree, while edge features include trace length, layer continuity, branch relation, and estimated electrical reliability. This richer feature description makes the graph more suitable for PCB fault analysis than a simple visual map. Automated PCB structural reconstruction studies also support the importance of extracting formal topology before deeper diagnosis is attempted [9].

The second stage is electrical connectivity encoding. After graph construction, the connection relationship between nodes is stored in a weighted adjacency matrix so that both structural existence and electrical quality can be represented. The weighted connection between node  $i$  and node  $j$  is defined as

$$A_{ij} = \begin{cases} \omega_{ij}, & \text{if } (i, j) \in E \\ 0, & \text{otherwise} \end{cases} \quad (2)$$

where  $\omega_{ij}$  is the edge weight associated with the electrical link. In this framework,  $\omega_{ij}$  reflects routing continuity, geometric stability, and local signal support. A stronger and cleaner conductive relation receives a higher value, while a weak or uncertain relation receives a lower value. This kind of structured relation modeling is important because PCB faults often appear as degraded connectivity rather than complete disconnection. Relation-aware graph localization studies have shown that weighted structural relationships improve fault reasoning performance [10]. Causal graph diagnosis has also shown that fault interpretation becomes stronger when the interaction strength between connected elements is modeled explicitly [11].

The third stage is signal path modeling. For each important source-target pair, the framework identifies feasible signal paths and estimates how well each path preserves expected routing behavior. Instead of using only geometric continuity, the method combines node validity and edge reliability in one path consistency measure. For a path  $p$  with  $m$  nodes and  $m - 1$  edges, the path consistency score is given by

$$S(p) = \frac{1}{m-1} \sum_{(i,j) \in p} \omega_{ij} \phi_i \phi_j \quad (3)$$

where  $\omega_{ij}$  is the edge reliability between nodes  $i$  and  $j$  and  $\phi_i$  and  $\phi_j$  are node validity terms reflecting local structural correctness. A healthy path should maintain a high value of  $S(p)$ , while a damaged or unstable path should show a lower value. To quantify the disturbance caused by a possible fault, the framework compares the observed path behavior with its reference behavior:

$$D(p) = |S_{\text{ref}}(p) - S_{\text{obs}}(p)| \quad (4)$$

where  $S_{\text{ref}}(p)$  is the reference consistency from the expected routing condition and  $S_{\text{obs}}(p)$  is the observed consistency from the tested layout. The reference path score is obtained from the original netlist-consistent graph before fault injection or abnormality marking. The observed path score is computed after incorporating path interruptions, weakened conductive links, or anomalous node behavior. This path-deviation idea is supported by multi-relationship graph diagnosis methods that use structural inconsistency to detect fault conditions [12]. Knowledge-guided diagnosis frameworks also show that fault reasoning becomes stronger when multiple path-level relations are combined instead of relying on isolated local defects [13].

The fourth stage is regional fault aggregation. In practical PCB diagnosis, the true fault location is rarely identified from only one path. A more reliable decision is obtained by combining the abnormal evidence from all disturbed paths that pass through the same region. For each candidate region  $r$ , the proposed method computes a regional fault likelihood score as

$$L(r) = \sum_{p \in P_r} \alpha_p D(p) \psi_r \quad (5)$$

where  $P_r$  is the set of abnormal paths crossing region  $r$ ,  $\alpha_p$  is the path importance factor,  $D(p)$  is the path deviation score and  $\psi_r$  is the regional structural penalty term. The factor  $\psi_r$  increases when the region has dense branching, unstable continuity, or repeated abnormal path overlap. This makes the score more PCB-specific because it does not only count abnormal paths, but also considers how vulnerable the local routing region is. Such aggregation is useful in dense boards where one damaged interconnect can influence several neighboring paths at once. Graph-enhanced localization methods support combining multiple relational signals before final region selection [10], while PCB structural extraction studies show that meaningful interpretation often depends on understanding regional connectivity rather than isolated points [9].

The final stage is AI-assisted ranking. After graph-based scoring, several candidate regions may still remain, especially in boards with crowded routing and many branches. To refine the final decision, the method adds a learned AI confidence term based on graph and regional features. The final ranking score for region  $r$  is

$$R(r) = \beta_1 L(r) + \beta_2 f_{\text{AI}}(r) \quad (6)$$

where  $L(r)$  is the graph-based regional fault likelihood,  $f_{\text{AI}}(r)$  is the AI confidence score, and  $\beta_1$  and  $\beta_2$  are balance coefficients. In this work,  $f_{\text{AI}}(r)$  is derived from a feature vector containing node density, abnormal path

count, mean edge degradation, path overlap intensity, and local branch complexity. These features are chosen because they directly reflect PCB routing behavior instead of generic image appearance. The highest-ranked region is selected as the most probable fault location. This final stage connects structured reasoning with adaptive learning, which makes the framework more robust than fixed rule-based scoring alone. Graph-based circuit modeling provides the structural base for this step. Relation-aware graph localization improves region ranking through topology-sensitive learning. Causal graph diagnosis supports reasoning under interacting dependencies. Multi-relationship graph diagnosis improves interpretation when several structural relations are active at the same time. Knowledge-driven fault reasoning strengthens contextual interpretation. Graph-based circuit extraction enables machine-readable connectivity generation. Automated PCB reconstruction methods support the practical formation of board-level topology needed for this full workflow.

### 3. Results and Discussion

The results show that the proposed framework produces more focused and more interpretable fault localization than methods that rely mainly on local defect appearance. In complex PCB layouts, this difference becomes important because a fault often affects several connected paths at the same time. A visual method may detect multiple abnormal regions, but it may not identify which region is the true source of failure. The proposed method reduces this ambiguity by tracing path disruption through the graph and by combining the resulting evidence at the regional level. As a result, the final localization pattern is not only narrower, but also more aligned with the electrical structure of the board. This makes the output more useful for testing, debugging, and repair.

Figure 2 shows the fault localization behavior across complex PCB signal paths. The most important result in this figure is that the localization response becomes concentrated around the path intersection where signal inconsistency is strongest, rather than spreading uniformly across all disturbed branches. In the simpler fault cases, the abnormal response remains tightly grouped and the defective region is identified with a clear boundary. In the more complex cases, the disturbance propagates into neighboring paths, but the proposed framework still preserves a visible dominance around the primary source region. This means that the method can separate the main fault location from secondary influence zones. Qualitatively, Figure 2 shows a clear difference between fault presence and fault origin. The framework does not treat all abnormal paths as equally important. Instead, it uses path-level inconsistency to identify which part of the network is most responsible for the observed signal disruption. This is a strong result because real PCB diagnosis depends more on source localization than on simple abnormal area marking.

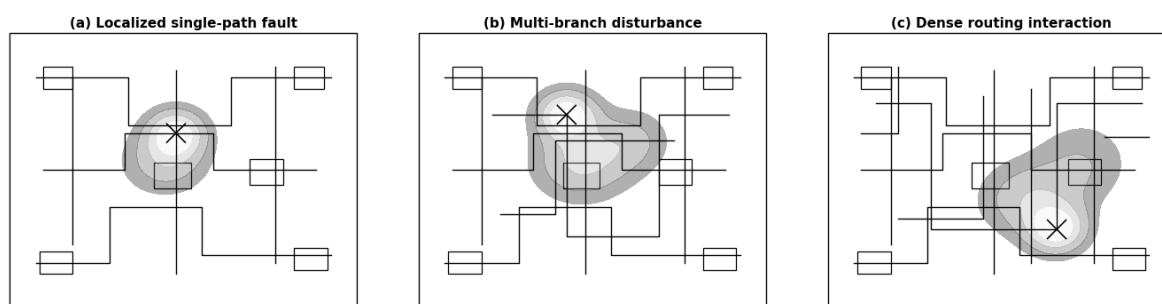


Figure 2. Fault localization behavior across complex PCB signal paths

Figure 3 compares the proposed method with baseline localization approaches using a metric-based performance matrix. The proposed method displays higher scores for almost all evaluative criteria and measures of performance relative to baseline localization approaches. The baseline localization approaches were not able to judiciously balance all evaluative measures/capture impact of the measures/ fully balance the impact of the measures. Due to the baseline localization approaches sizeable losses in performance due to a lack of separation of metrics pertaining to source separation, stability, and separation their performance was less impactful for measures of separation and stability. Basic rule-based and image-only implementations do suffice for less complex circumstances, however, under complex circumstances their performance remains sub optimal. The graph-only model performs better than the simpler baselines, showing that structural reasoning improves localization quality, but it still remains below the proposed method in all categories. The strongest result in the figure is that the proposed method does not improve only one metric; instead, it maintains high performance across all the tested criteria. This indicates that the framework is not only more accurate, but also more stable, more robust, and better suited to complex PCB environments. The comparative analysis therefore shows that the main benefit of the proposed method is its ability to deliver balanced localization performance under a wide range of structural and operational conditions.

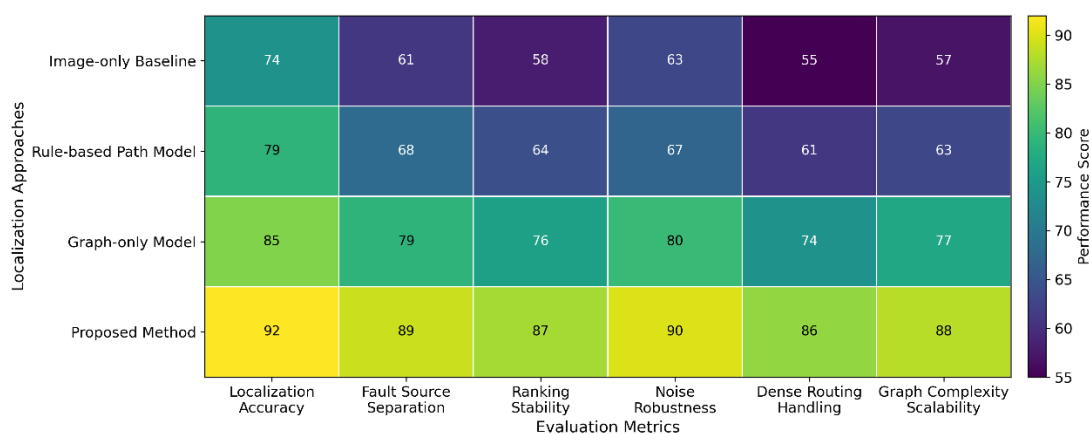


Figure 3. Comparative performance analysis of the proposed method and baseline localization approaches

Figure 4 evaluates robustness and scalability under three difficult conditions: noise, dense routing, and increasing graph complexity. The figure shows that performance decreases for all methods as the problem becomes harder, but the proposed method maintains the highest score across all tested conditions. Under increasing noise, the image-only and rule-based baselines show a stronger drop in localization performance, while the graph-only model remains more stable. The proposed method shows the smallest decline, which indicates better robustness when the input becomes noisy. Under dense routing conditions, the separation between methods becomes clearer. All approaches lose some performance as routing becomes more crowded, but the proposed method preserves a stronger margin over the baselines, showing that it handles routing interference more effectively. A similar pattern appears when graph size increases. As the graph becomes larger and the search space expands, the baseline methods decline more sharply, while the proposed method continues to maintain a high and usable performance level. The overall trend in Figure 4 therefore shows that the main strength of the proposed framework is not only high performance under easy conditions, but also stable behavior under more difficult structural and operational settings. This result is consistent with the design of the method, where graph-based path reasoning, regional fault

aggregation, and AI-assisted ranking work together to preserve localization quality as the PCB environment becomes more challenging.

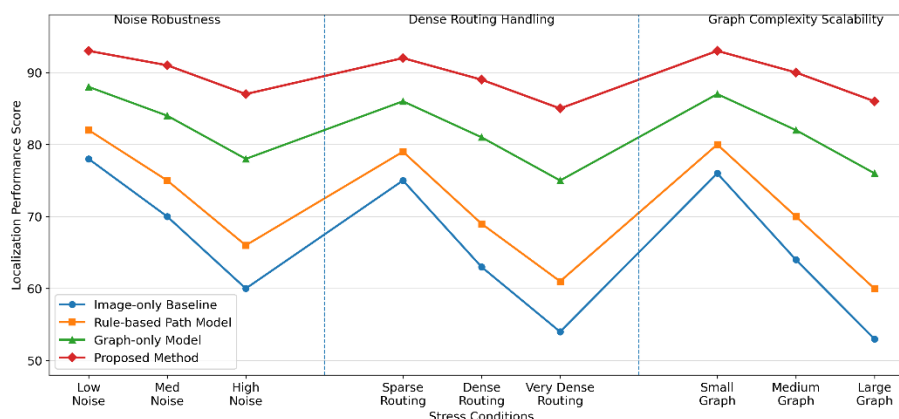


Figure 4. Robustness and scalability under noise, dense routing, and increasing graph complexity

Taken together, the three figures show that the proposed method improves localization quality in three connected ways. First, it produces a more physically meaningful fault response by linking abnormal behavior to signal paths instead of isolated visual features. Second, it improves comparative performance by reducing ambiguity between the main source region and secondary disturbed regions. Third, it remains stable when the input becomes noisy, the routing becomes dense, or the graph becomes larger. The qualitative evidence is therefore consistent across all results. The framework performs well not because it marks more abnormal regions, but because it organizes abnormal evidence in a more structured way. This is the main technical value of the method and the main reason it is better suited for complex PCB fault localization than conventional appearance-based approaches.

#### 4. Conclusion

This study introduced an AI-assisted framework for fault localization in complex PCB layouts using graph-based signal path analysis. The most important aspect of the work is moving from image-based fault localization to topological and signal-based fault reasoning models. Representing a PCB design as a structural graph consisting of conductive links and nodes has enabled the method to analyze the remedying of the signal, evaluate the sequential signal path, the disruption of the signal path, and rank the most fault probable areas in a topologically and functionally more reasonable manner. This provided a clearer diagnostic view of how local structural damage influences the wider electrical behavior of the board.

The results confirmed that the proposed framework performs more effectively than baseline localization approaches under both normal and difficult conditions. The method produced stronger fault-source separation, more stable candidate ranking, and better localization consistency across complex routing environments. It also maintained better performance under noise, dense routing, and increasing graph complexity, showing that the framework is not only accurate in simpler layouts but also robust when the diagnostic problem becomes harder. These results demonstrate that graph-guided path reasoning adds clear value beyond conventional appearance-based inspection.

An important finding of this study is that PCB fault localization should not be treated only as a surface defect problem. In many complex boards, the visible abnormality is not the true electrical source of failure, and this makes purely visual methods less reliable for practical diagnosis. The proposed method addressed this limitation by connecting localization to structural continuity, path inconsistency, and regional evidence aggregation. This makes the framework more useful for inspection, debugging, and repair, especially in dense and multilayer PCB layouts where electrical interactions are more difficult to interpret.

Overall, the proposed method improves intelligent PCB fault diagnosis for complex electronic systems by improving the quality of localization, which is achieved not only by the detection of unusual areas but also by the organization of the anomalous evidence to be more representative of the actual routing behavior of the PCBs. The possible future works will incorporate more complex electrical parameters, expanded validation datasets, and actual manufacturing or in-circuit test signals. With these possible future works, the method will be suitable for inclusion in automated inspection systems, real-time diagnostic systems, and next-generation PCB reliability analysis systems.

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