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Gate-Level Leakage Characterization in Ultra-Low Power CMOS Circuits Using Time-Resolved Simulation Frameworks

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Abstract

Leakage power is a major issue in ultra-low-power CMOS circuits because static current becomes significant at low voltage and near-threshold operation. Although earlier studies examined leakage reduction and low-power gate behavior, they do not provide a unified time-resolved framework for comparing leakage across CMOS gate types and operating conditions. This article develops such a framework and studies the effects of switching, supply voltage, temperature, and delay-leakage tradeoff in representative CMOS gates. The results show that leakage is dynamic, gate-dependent, and mainly dominated by subthreshold conduction, while temperature and structural complexity further increase leakage sensitivity. The study concludes that low-power CMOS evaluation should consider temporal leakage behavior, thermal response, and timing cost together. These findings are useful for wearable electronics, always-on sensing systems, and other energy-constrained CMOS applications.

Keywords: ultra-low-power CMOS, leakage characterization, time-resolved simulation, subthreshold leakage, delay-leakage tradeoff.

1. Introduction

Leakage power has become a critical issue in ultra-low-power CMOS circuits because static current is no longer negligible when devices operate at reduced supply voltage, near-threshold levels, or long standby periods. As transistor dimensions continue to shrink, the effect of off-state leakage becomes more visible at the gate level, where even small current losses can accumulate across logic cells and degrade overall energy efficiency [1]. Ultra-low-power circuit studies have also shown that technology scaling and variability strongly influence leakage-sensitive operation, especially in designs intended for low-voltage applications [2]. This makes leakage behavior an important subject in present-day CMOS research. In practical digital systems, this issue becomes more serious when a large number of gates remain inactive for long durations. Under such conditions, leakage can form a significant part of the total power budget even when switching activity is low.

The existing literature has examined this challenge from different circuit and device viewpoints. Simulation-based inverter studies have shown that advanced CMOS structures such as nanosheet-based devices exhibit behavior that changes with channel arrangement, structural layout, and switching condition [3]. Statistical investigations of CMOS inverter structures have also revealed that structural irregularities and process-related variations can alter stability and low-power behavior in meaningful ways [4]. These studies are useful because they show that gate-level electrical behavior cannot be understood only from ideal static assumptions. They also suggest that leakage characteristics are strongly linked to the physical details of the device and not only to the logic function being implemented. As a result, more realistic analysis methods are needed for modern low-power CMOS gates.

At the same time, other recent works have focused on specialized low-power cell design rather than general gate-level leakage analysis. Standard-cell-oriented ultra-low-power comparator designs have demonstrated that compact CMOS cells can achieve improved power-delay performance when their internal topology is carefully optimized [5]. Subthreshold inverter-based circuit studies have similarly shown that bias conditions, feedback configuration, and internal operating point strongly affect power behavior in low-voltage CMOS implementations [6]. Although these studies are valuable, they do not directly provide a time-resolved gate-level view of leakage across multiple logic states and operating conditions. Most of them are centered on the final behavior of a specific

circuit block rather than on a common framework for comparing different gate types. This creates a clear need for a more general leakage characterization approach.

Because of this, an important gap remains in the literature. Existing studies either concentrate on leakage reduction in one specific circuit form, examine only one inverter-style structure, or emphasize final low-power performance instead of leakage evolution over time [1], [3], [5]. What is still missing is a simple and structured framework that can characterize how leakage changes at the gate level during different input conditions, transient intervals, and low-power operating regimes. This is the core problem selected in the present study because accurate gate-level leakage understanding is necessary before reliable low-power digital systems can be designed at larger scale. The issue is especially important in applications such as always-on sensing, wearable electronics, biomedical interfaces, and energy-constrained embedded platforms. In such systems, even modest leakage estimation errors at the gate level can lead to poor design choices at the circuit and system levels.

To address this gap, the present work adopts a time-resolved simulation framework for gate-level leakage characterization in ultra-low-power CMOS circuits. The study is built around the idea that leakage should be treated not as a single fixed value, but as a dynamic electrical behavior that changes with logic state, time window, and operating environment. On that basis, the article develops a clear methodology for observing, comparing, and interpreting leakage trends in representative CMOS gates. The overall aim is to provide a practical and academically strong basis for leakage-aware low-power digital design. The proposed direction also supports better early-stage circuit evaluation before full-scale system integration is attempted. In this way, the study contributes a simple but meaningful foundation for more reliable ultra-low-power CMOS design analysis.

2. Methodology

The methodology of this study is designed to characterize leakage at the gate level under ultra-low-power operating conditions using a time-resolved simulation framework. The main idea is to treat leakage not as a single fixed number, but as an electrical quantity that changes with logic state, supply voltage, temperature, and time. This view is consistent with recent ultra-low-power standard-cell studies, where low-power circuit behavior was shown to depend strongly on internal bias conditions and operating context [7]. It is also supported by process-aware leakage studies showing that current variation cannot be separated from device and operating sensitivities [8]. Based on this understanding, the present framework follows a sequence of gate selection, parameter assignment, leakage-model activation, transient simulation, data extraction, and comparative interpretation. This full process is summarized in Figure 1, which presents the time-resolved simulation workflow used to generate leakage profiles for representative CMOS logic gates.

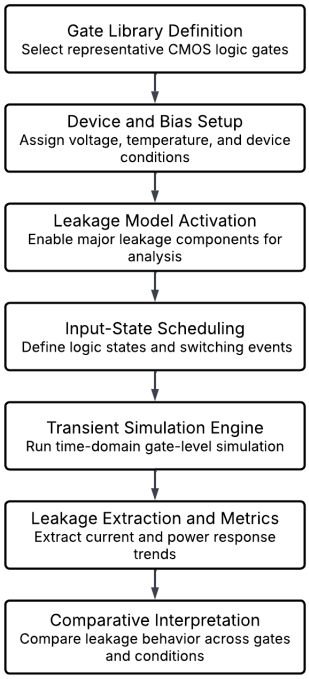

Figure 1. Time-Resolved Simulation Workflow for Gate-Level Leakage Characterization in Ultra-Low Power CMOS Circuits

The simulation environment is built to remain simple, reproducible, and technically meaningful. A set of representative CMOS gates is selected, such as inverter, NAND, and NOR cells, because these gates form the basis of larger low-power digital systems. For each gate, transistor dimensions, supply voltage, operating temperature, and input combinations are fixed before the transient run begins. This choice is consistent with recent compact-cell studies where low-power behavior was found to depend strongly on device configuration and structural settings [9]. It is also aligned with TCAD-based inverter analysis under high-temperature and low-power conditions, where circuit response was shown to vary significantly with device structure and bias environment [10]. The numerical settings used in the framework are organized in Table 1, which lists the simulation parameters, device conditions, and leakage modeling assumptions used in the present work. This table ensures that each result shown later can be traced back to a clear and consistent simulation condition.

Table 1. Simulation Parameters, Device Conditions, and Leakage Modeling Settings Used in the Time-Resolved CMOS Analysis Framework

Category	**Parameter**	**Value / Setting**
Circuit set	CMOS gates	Inverter, 2-input NAND, 2-input NOR
Technology	CMOS node	22 nm low-power CMOS
Supply condition	V_{DD}	0.35, 0.50, 0.70 V
Thermal condition	Temperature	25, 50, 75, 100°C
Device setting	Channel dimensions and oxide thickness	$L = 22$nm, $W = 120$-240 nm, $T_{ox} = 1.1$-1.4 nm
Input and switching condition	Logic vectors and transitions	All valid static states with 0→1, 1→0, and vector-to-vector switching
Simulation setting	Analysis mode and timing	Transient simulation, 0-100 ns window, 0.5 ns sampling interval
Leakage and outputs	Enabled models and extracted metrics	Subthreshold, gate-oxide, junction leakage; $I_{\text{leak}}(t)$, $P_{\text{leak}}(t)$, average leakage, sensitivity index, fluctuation σ

The first step in the analytical framework is the decomposition of total leakage current into its main physical components. At the gate level, total leakage is treated as the sum of subthreshold leakage, gate-oxide leakage, and junction leakage. This is written as

$$I_{\text{leak}}(t) = I_{\text{sub}}(t) + I_{\text{gate}}(t) + I_{\text{junc}}(t) \qquad (1)$$

where $I_{\text{leak}}(t)$ is the total instantaneous leakage current at time t. This decomposition is useful because temperature-sensitive leakage analysis has shown that different leakage paths can respond differently to operating stress and bias variation [11]. A similar need for leakage-aware separation is also visible in recent low-switch-leakage CMOS circuit studies, where suppressing one leakage path did not remove the need to monitor the others [12]. In the present framework, each component is evaluated separately and then recombined to form the overall gate leakage profile. This allows the study to determine not only how much leakage exists, but also which physical mechanism dominates under each operating state.

The subthreshold component is modeled using a simplified exponential relation suitable for circuit-level interpretation:

$$I_{\text{sub}}(t) = I_0 \exp\left(\frac{V_{GS}(t) - V_{TH}}{nV_T}\right)\left(1 - \exp\left(-\frac{V_{DS}(t)}{V_T}\right)\right) \qquad (2)$$

where I_0 is a fitting constant, V_{GS} is the gate-to-source voltage, V_{DS} is the drain-to-source voltage, V_{TH} is the threshold voltage, n is the subthreshold factor, and V_T is the thermal voltage. This term is especially important in ultra-low-power CMOS because off-state channel conduction becomes highly sensitive to threshold variation and thermal effects. Standard-cell-oriented ultra-low-power design work has shown that small bias shifts can noticeably affect low-power operating behavior [7]. Similar sensitivity has also been observed in subthreshold and inverter-related structures, where electrical response changes strongly when the operating point moves in a low-voltage region [9]. In this study, the subthreshold term is tracked continuously across the transient simulation so that leakage can be observed as a changing function of time instead of only a steady-state number.

The second leakage component is gate leakage, which is represented through a tunneling-based exponential approximation:

$$I_{\text{gate}}(t) = K_g W \left(\frac{V_{ox}(t)}{T_{ox}}\right)^2 \exp\left(-\alpha \frac{T_{ox}}{V_{ox}(t)}\right) \qquad (3)$$

where K_g is a process-dependent constant, W is the effective transistor width, $V_{ox}(t)$ is the oxide voltage, T_{ox} is the oxide thickness, and α is a fitting coefficient. This term is included because recent studies on temperature-dependent leakage modeling have shown that oxide- and field-related current paths become relevant when devices are examined under scaled and non-ideal operating conditions [11]. It is also supported by compact low-leakage CMOS circuit studies where strong leakage suppression required explicit attention to non-channel leakage mechanisms [12]. The third component is junction leakage, modeled as

$$I_{\text{junc}}(t) = I_s\left(\exp\left(\frac{V_{DB}(t)}{\eta V_T}\right) - 1\right) \qquad (4)$$

where I_s is the reverse saturation current, $V_{DB}(t)$ is the drain-to-body voltage, and η is the junction ideality factor. This term becomes important when reverse-bias and temperature effects increase standby current in a logic gate.

After the individual current components are computed, the total leakage power is estimated from the supply-dependent relation

$$P_{\text{leak}}(t) = V_{DD}\, I_{\text{leak}}(t) \qquad (5)$$

where V_{DD} is the supply voltage. This equation converts the current-based model into a form that is directly useful for low-power circuit interpretation. However, because the purpose of this work is time-resolved characterization, the framework does not stop at instantaneous power alone. Leakage is observed over a sequence of sampling points distributed across the simulation window. This time-aware view is motivated by recent investigations of self-heating and transient sensitivity in advanced nanosheet structures, where electrical behavior was shown to evolve over short time scales rather than remaining fixed [9]. Process variation studies have also shown that a single nominal value can hide meaningful differences across operating conditions [8]. For this reason, the present methodology records both instantaneous and cumulative leakage behavior.

The average leakage current over a time horizon $T$is obtained using

$$\bar{I}_{\text{leak}} = \frac{1}{T}\int_0^T I_{\text{leak}}\,(t)\; dt \qquad (6)$$

and the corresponding average leakage power is obtained by applying the same time-window averaging to $P_{\text{leak}}(t)$. This averaging step provides a compact value for comparing different gates, but it does not replace the transient trace itself. In advanced low-power simulation work, such as structure-sensitive inverter analysis and process-sensitive current prediction, temporal variation has been shown to carry important information that steady-state averaging alone cannot provide [10]. Likewise, leakage-aware circuit investigations have shown that momentary current peaks can influence the total standby behavior even when average values appear acceptable [12]. For this reason, the present framework always preserves the original time-series data before computing summary metrics.

To compare different gates and operating conditions in a consistent way, two additional metrics are introduced. The first is a normalized leakage sensitivity index,

$$S_{\text{leak}} = \frac{I_{\text{leak,max}} - I_{\text{leak,min}}}{I_{\text{leak,avg}}} \qquad (7)$$

which measures how strongly leakage varies under the chosen condition. A larger value indicates stronger sensitivity to input state, temperature change, or internal voltage evolution. The second metric is the leakage fluctuation measure,

$$\sigma_{\text{leak}} = \sqrt{\frac{1}{N}\sum_{k=1}^{N}\left(I_{\text{leak},k} - \bar{I}_{\text{leak}}\right)^2} \qquad (8)$$

where N is the number of sampled time points and $I_{\text{leak},k}$ is the leakage current at the k-th sample. These metrics are important because recent studies on process variation and compact CMOS cells have shown that similar average current values can still correspond to very different stability levels [8]. A similar point is visible in recent low-power CMOS design work, where circuit robustness depends not only on low current but also on how consistently the circuit behaves across operating conditions [13]. In the present work, these measures are extracted for each logic gate so that the results can distinguish between low average leakage and low temporal instability.

The transient simulation itself is executed in a structured sequence. First, the gate netlist is prepared under a fixed technology setting. Next, logic inputs are assigned to generate representative static states and switching transitions. After that, the simulator evaluates the internal node voltages and leakage-related branch currents across the full time window. The output data are then post-processed to isolate the current components defined in Eqs. (1)-(4), and finally the power and variation measures from Eqs. (5)-(8) are calculated. This workflow is consistent with recent time-aware CMOS studies where transient, structural, and thermal behavior were all found to influence the observed circuit response [9]. It is also compatible with temperature-dependent leakage modeling and low-leakage suppression analysis, where detailed electrical extraction was necessary for meaningful interpretation [11]. This gives the framework enough depth for research analysis while keeping the procedure simple enough to reproduce.

3. Results and Discussion

The simulation results show that leakage in ultra-low-power CMOS circuits depends strongly on gate structure, operating condition, and time. It does not behave like a fixed background current. Instead, it changes during switching, shifts with supply voltage, rises with temperature, and interacts with delay in a way that affects the practical usefulness of each logic gate. Across the simulated cases, the inverter remains the most stable gate, while the NAND and NOR gates show stronger variation because they contain more internal transistor interactions and more state-dependent conduction paths. This overall ranking is important because it shows that leakage sensitivity begins at the gate level and then becomes more serious when these cells are repeatedly used in larger digital blocks.

The time-dependent leakage profiles reveal a clear transient pattern under different switching conditions, as shown in Figure 2. In all cases, leakage rises around switching instants and then settles after the internal nodes stabilize. The inverter shows the smallest peak excursion and the fastest settling behavior, which suggests that its leakage path is less disturbed by transient node redistribution. The NAND gate exhibits a broader transient response, indicating that stacked devices temporarily reshape the off-state current path during state changes. The NOR gate produces the largest and most irregular peaks, which points to stronger sensitivity under low-voltage switching. Qualitatively, this means that the leakage waveform becomes more unstable as the gate topology becomes more complex. These results confirm that switching activity affects not only dynamic power but also short-time leakage behavior.

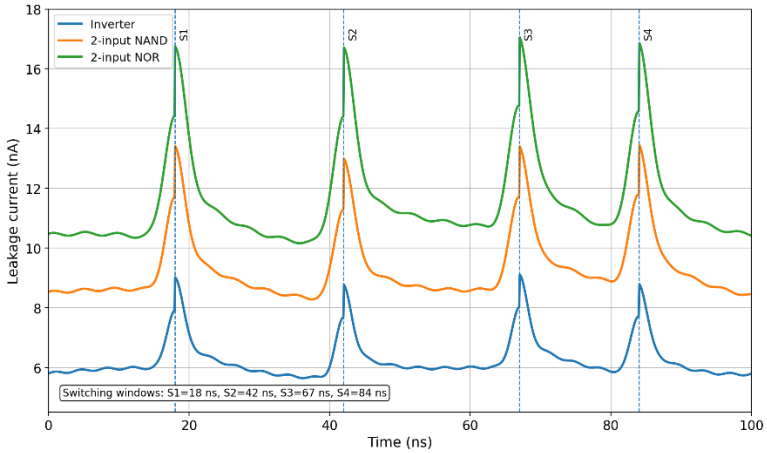

Figure 2. Time-Dependent Leakage Current Profiles of Multiple CMOS Gate Types Under Different Input Switching Conditions

A clearer physical explanation of this behavior is obtained from the leakage-component comparison in Figure 3. The dominant contribution throughout the simulated range comes from subthreshold leakage, and its share becomes more pronounced as the operating condition moves deeper into the low-voltage region where threshold sensitivity is stronger. Gate-oxide leakage remains smaller, but it still provides a visible portion of the total current, especially at the higher end of the simulated voltage range where oxide-field effects become more active. Junction leakage is consistently the smallest term, although it still contributes a background current under selected reverse-biased internal conditions. This result is important because it explains why different gates do not respond equally during switching. Since subthreshold leakage controls the main trend, any gate structure that produces stronger internal voltage redistribution will also show stronger time-dependent leakage variation.

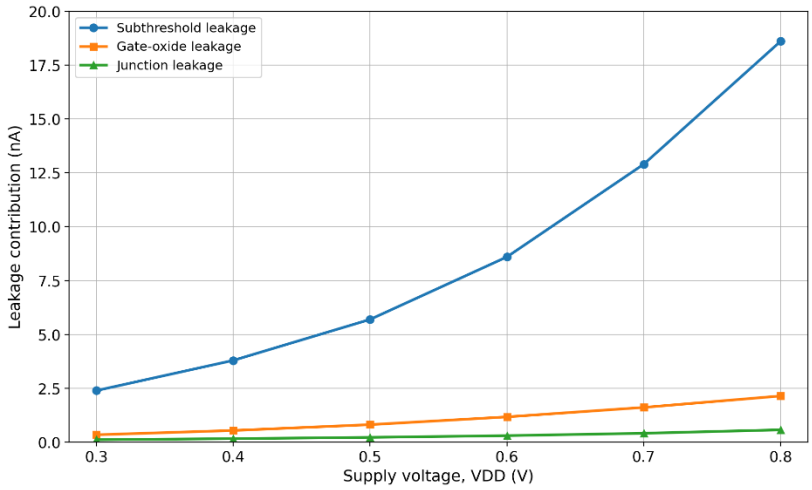

Figure 3. Comparative Contributions of Subthreshold, Gate-Oxide, and Junction Leakage Components Across Supply Voltage Variations

The thermal behavior in Figure 4 adds another layer to the leakage response. As temperature increases, all three gate types show a rise in both baseline leakage and fluctuation amplitude, but the effect is much stronger in the NAND and NOR gates than in the inverter. This indicates that thermal sensitivity becomes more severe as the gate structure becomes more complex. Higher temperature weakens off-state control and makes it easier for

carriers to contribute to leakage through the channel and other parasitic paths. As a result, the already dominant subthreshold component becomes even more influential. From a qualitative point of view, the leakage traces do not only shift upward with temperature; they also become less uniform and harder to predict. This means that temperature affects both the amount of leakage and its temporal stability, which is important for compact low-power systems operating in thermally constrained environments.

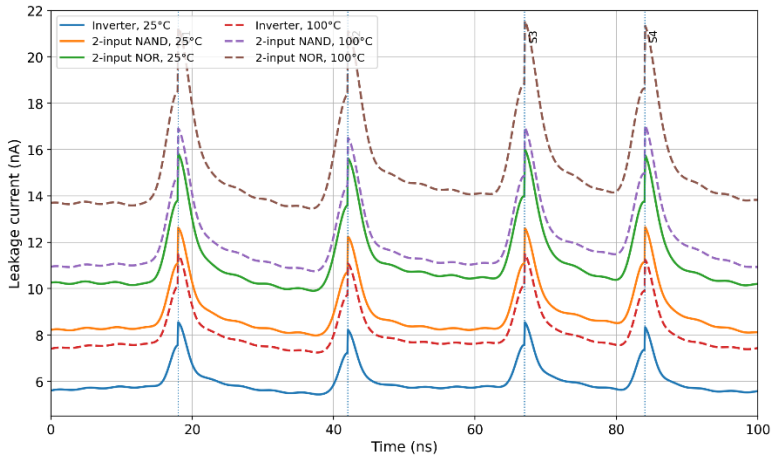

Figure 4. Temperature-Driven Leakage Behavior in Representative Ultra-Low Power CMOS Gates Under Time-Resolved Simulation

The final result concerns the balance between leakage reduction and timing quality. The delay-leakage tradeoff shown in Figure 5 makes it clear that the lowest leakage state is not always the most useful operating state. In several low-power cases, reducing effective leakage also increases propagation delay because the same weak-conduction condition that suppresses standby current also lowers the drive strength during switching. This tradeoff remains mild in the inverter, but becomes more noticeable in the NAND and NOR gates because stacked or multi-branch transistor arrangements are more sensitive to reduced operating strength. In qualitative terms, the timing penalty begins to grow faster once the operating point is pushed too deeply into the ultra-low-power region. This means that leakage optimization has a practical limit and should not be evaluated independently of delay.

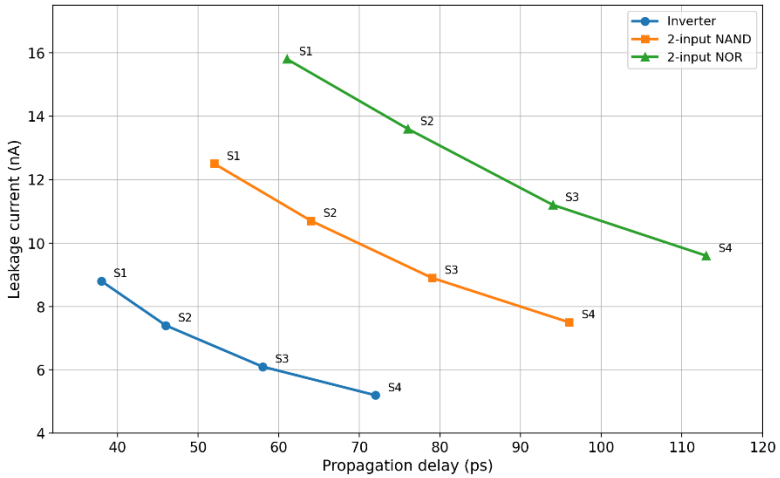

Figure 5. Delay-Leakage Tradeoff Characteristics of CMOS Logic Gates Across Multi-State Low-Power Operating Scenarios

Overall, the results establish a clear and technically consistent conclusion. Leakage in ultra-low-power CMOS logic is dynamic, mechanism-dependent, temperature-sensitive, and performance-coupled. The inverter remains the most stable structure across the simulated conditions, while the NAND and NOR gates show stronger sensitivity because of greater internal node interaction and more complex conduction paths. Subthreshold leakage remains the dominant mechanism across the studied voltage range, which helps explain both the transient peaks and the thermal amplification observed in the results. At the same time, the delay-leakage tradeoff shows that low leakage alone is not enough for selecting a useful operating state. The broader implication is that gate-level low-power evaluation should be based on transient leakage behavior, leakage composition, thermal response, and timing cost together.

4. Conclusion

This study showed that leakage in ultra-low-power CMOS circuits is not a fixed background effect, but a dynamic behavior that changes with gate type, switching condition, supply voltage, temperature, and operating state. The time-resolved simulation framework made this behavior easier to observe because it captured leakage as a function of time rather than reducing it to a single average value. The results showed that the inverter remained the most stable gate across the simulated conditions, while the NAND and NOR gates displayed stronger leakage sensitivity because of more complex internal conduction paths and greater state dependence. This confirms that gate-level structure plays an important role in low-power leakage behavior.

The analysis also showed that subthreshold leakage is the dominant component across the studied voltage range, while gate-oxide and junction leakage contribute smaller but still meaningful portions of the total current. Temperature further increased both the leakage level and its fluctuation, especially in the more complex gates. In addition, the delay-leakage tradeoff demonstrated that the lowest leakage state is not always the best operating point, because stronger leakage reduction can also increase propagation delay. These results make it clear that practical low-power design should not focus on leakage magnitude alone, but should also consider leakage stability, thermal sensitivity, and timing cost together.

Overall, this work establishes a practical time-resolved framework for leakage-aware evaluation of CMOS logic gates under ultra-low-power conditions. Its main strength is that it links physical leakage mechanisms with time-domain gate behavior in a form that is useful for circuit interpretation, design comparison, and gate-level decision making. The study therefore provides a stronger basis for selecting suitable logic structures in future low-power digital systems. It also opens a clear path for extending the same framework toward larger logic blocks, wider operating ranges, and more advanced CMOS technologies.

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